

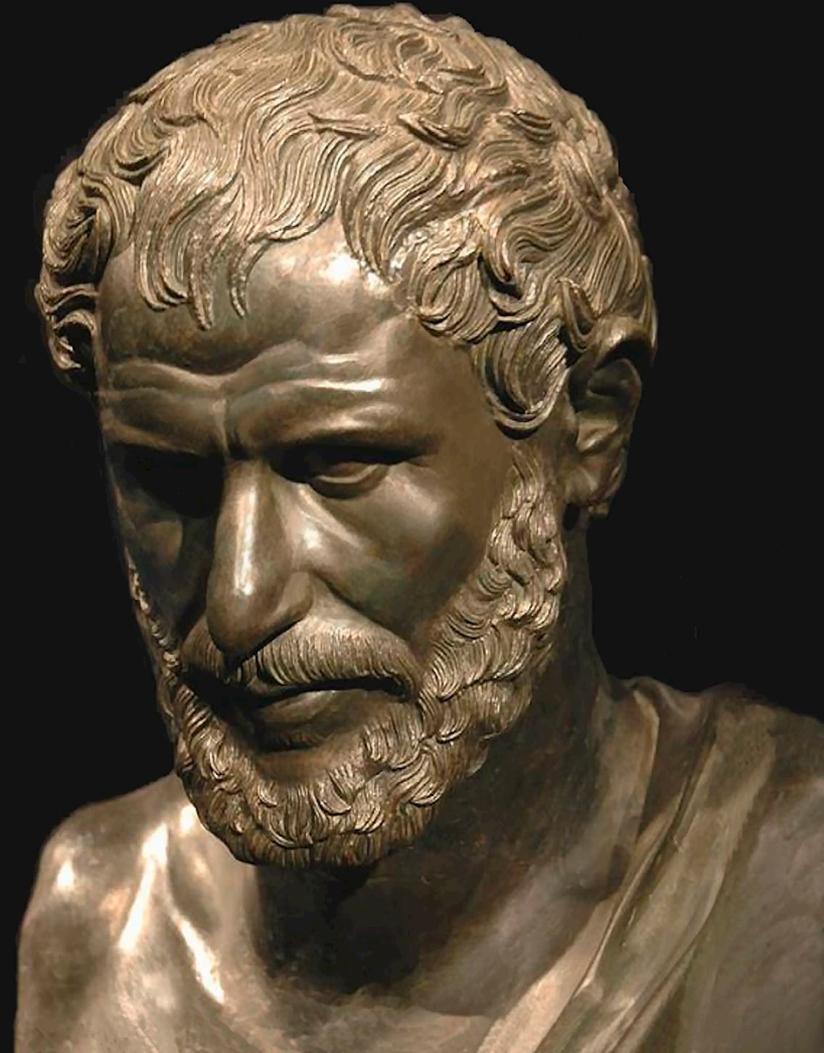


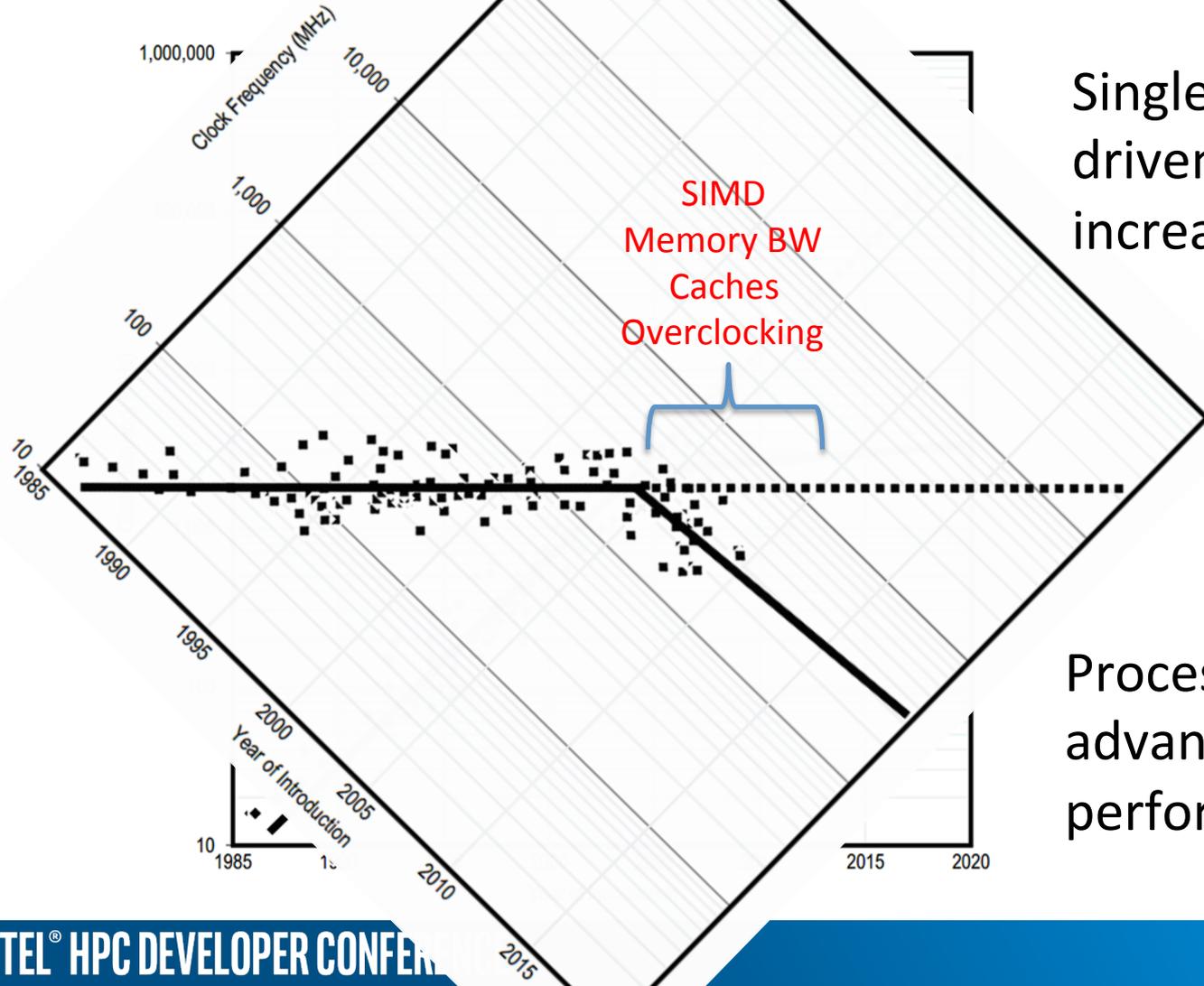
Success Through Community

Richard Gerber
NERSC HPC Department Head
NERSC Senior Science Advisor
President, Intel Xeon Phi Users Group

“The only thing constant is change”

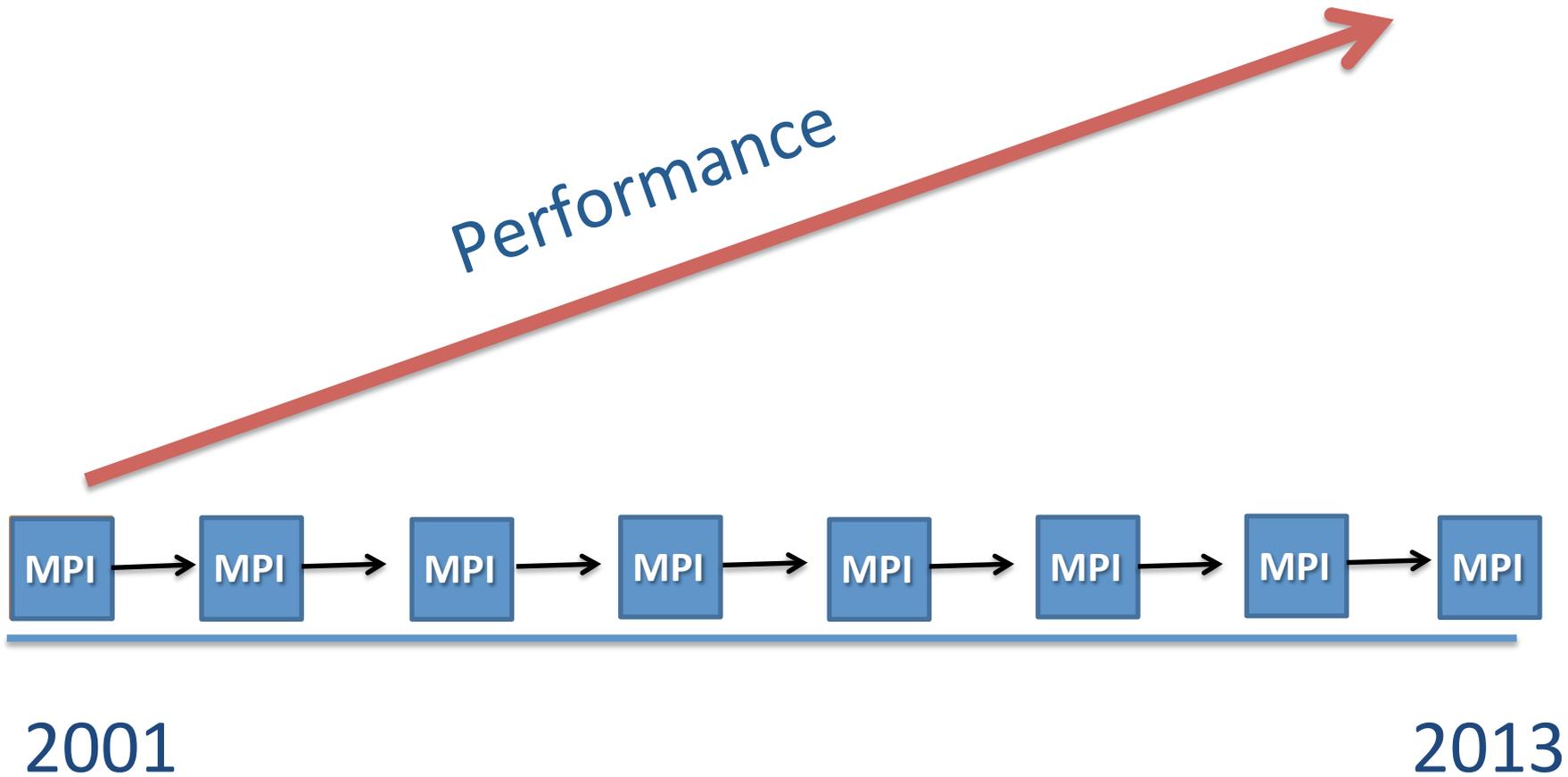
—Heraclitus of Ephesus



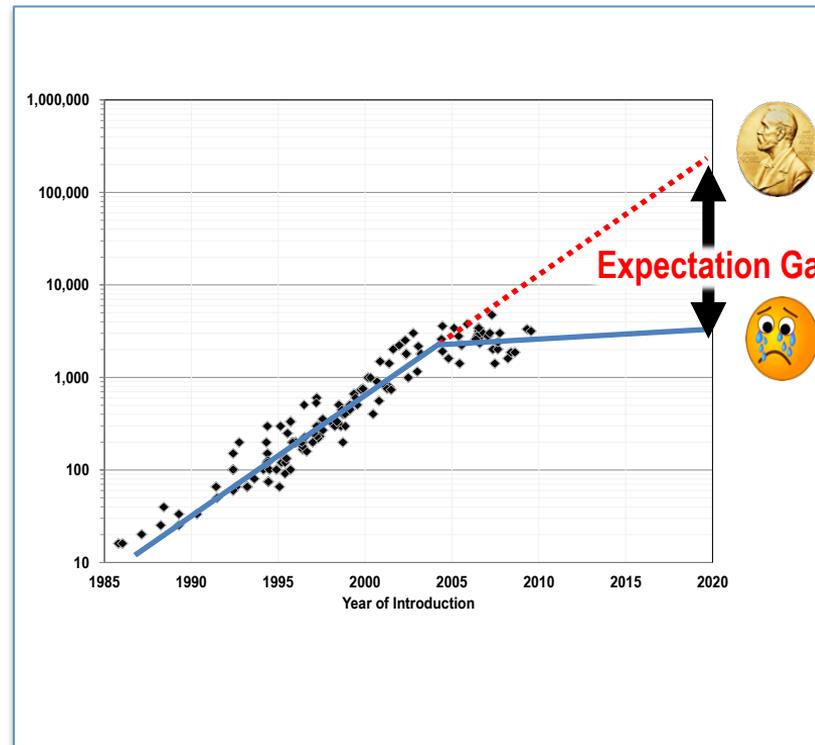
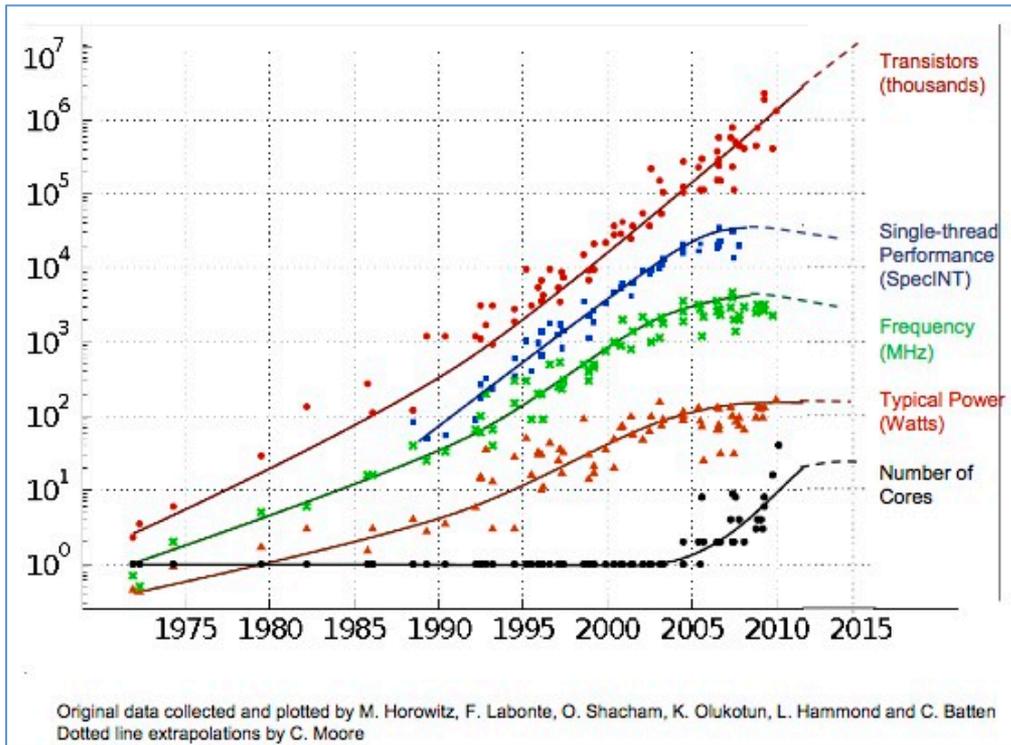


Single-CPU performance
driven by clock
increasing frequency

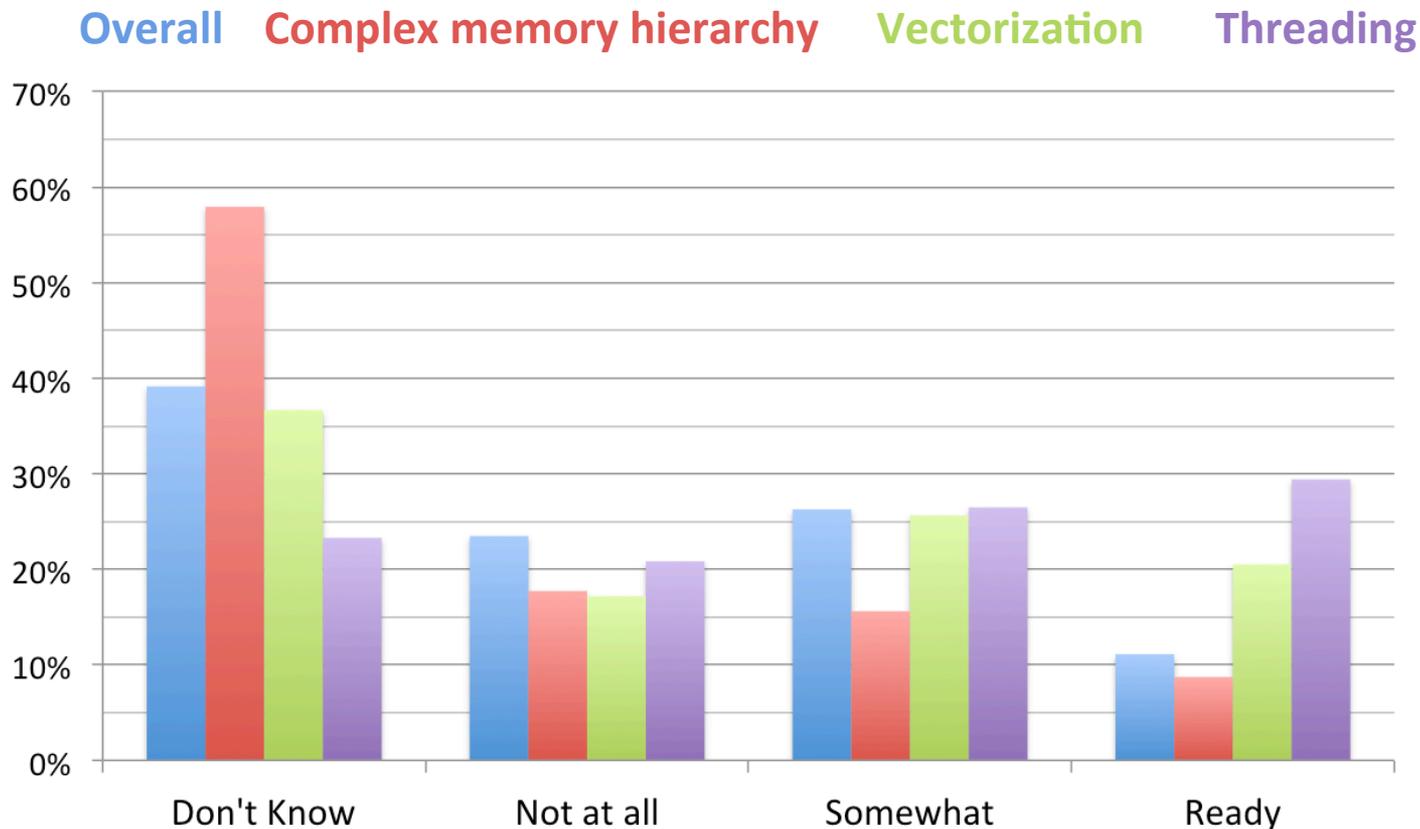
Processor, memory
advances kept CPU core
performance strong



Change was coming and we kept telling our 6,000 users it was so ...



NERSC User Survey 2013-14: Is Your Code Ready for Manycore?



We don't choose our users or codes. We support all DOE mission science.



2.4 Pflop Cray XC30 thrills NERSC's 6,000 users with 5,400 nodes, 100 GB/s memory bandwidth, and 2.4 GHz Intel Xeon "Ivy Bridge" processors, Cray Aries interconnect

"Edison is one of the best machines in the world," NERSC 2014 User Survey

2014 Top 500 Supercomputers

Rank	System	Processor
1	Tianhe-2	Intel Xeon Phi
2	Titan	NVIDIA K20x
3	Sequoia	BG/Q
4	K Computer	SPARC 64
5	Mira	BG/Q
6	Piz Daint	NVIDIA K20x
7	Stampede	Intel Xeon Phi
8	JUQUEEN	BG/Q
9	Vulcan	BG/Q
10	Cray CS-Storm	NVIDIA K40

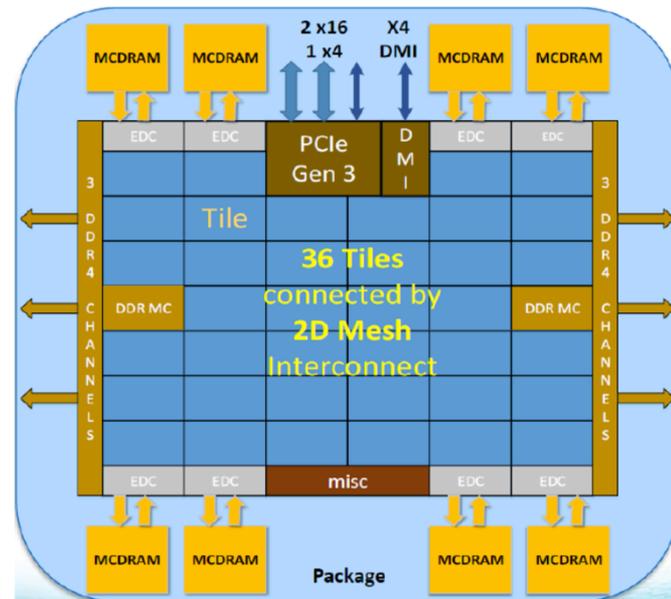
lightweight cores

NERSC to Procure "Cori" a Knights Landing Based Cray XC Supercomputer

May 2, 2014 by Rob Farber — [Leave a Comment](#)

30 PFlop System will be a boon to science because of new capabilities, but the Intel Xeon Phi many-core architecture will require a code modernization effort to use efficiently.

For the first time, NERSC's users will have lower single-thread performance in their next system.







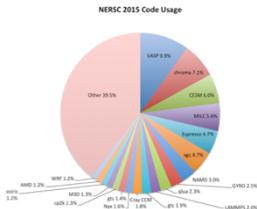
NERSC's Challenge

Prepare NERSC's diverse community of 6,000 users, 750 projects, and 700 codes to use Cori's Intel Xeon Phi Knights Landing processors at high performance

Business as usual was over

Solution: Build a Connected Community

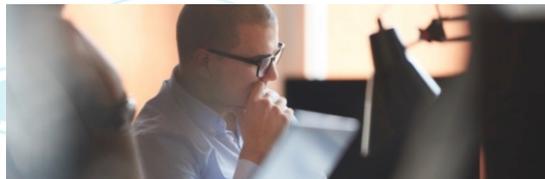
NESAP: 20 codes, >50% workload



NERSC Application Performance Team
Staff & Postdocs

IXPUG
THE INTEL XEON PHI USERS GROUP

Community Confluence



Robust training programs
~100s –1,000s of users



Computational Scientists

NESAP is Busily Using Dungeons to Slay Code Dragons
By John Russell

NESAP, Intel, Cray

Intel Software Developer Zone

MODERN CODE Home

Intel Parallel Computing Centers (Intel PCC)

FUEL YOUR INSIGHT: INTEL HPC DEVELOPER CONFERENCE 2016
November 12-13, 2016 - Salt Lake City





Optimization of scientific applications
Forum for free exchange of information and ideas
Collaboration among community experts
Independent projects, globally shared knowledge

Member Locations & Events



Monthly Working Groups

General Optimization
& Tuning



John Pennycook
john.pennycook@intel.com

Vectorization



Georg Zitzlsberger
georg.zitzlsberger@intel.com

MPI



Michael Lysaght
michael.lysaght@ichec.ie

Join, attend and/or host a meeting!

www.ixpug.org/working-groups

The Payoff: Performance



Original
Xeon Phi



Original
Haswell



Optimized
Haswell



NERSC
Xeon Phi Target



Optimized
Xeon Phi



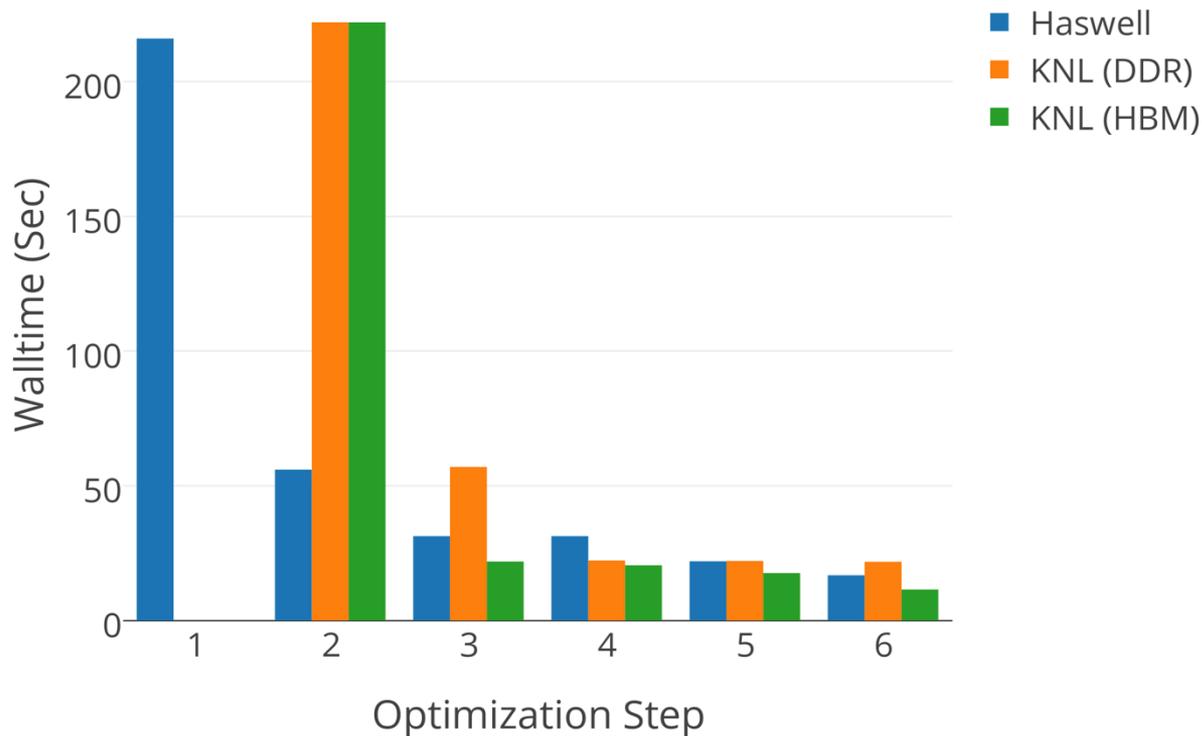
Performance
Rock Stars



BerkeleyGW Optimization Example

Sigma Optimization Process

1. Refactor (Create loops ready for OpenMP, vector optimizations)
2. Add OpenMP
3. Initial Vectorization (loop reordering, conditional removal)
4. Cache-Blocking
5. Improved Vectorization
6. Hyper-threading





We're published!

IXPUG

Application Performance on Intel Xeon Phi – Being Prepared for KNL and Beyond 304
Richard A. Gerber, Kent Milfeld, Chris J. Newburn, and Thomas Steinke

A Comparative Study of Application Performance and Scalability on the Intel Knights Landing Processor 307
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Tareq Malas, Thorsten Kurth, and Jack Deslippe

LNCS 9945

High Performance Computing

ISC High Performance 2016 International Workshops
ExaComm, E-MuCoCoS, HPC-IODC, IXPUG, IWOPH, P'3MA, VHPC, WOPSSS
Frankfurt, Germany, June 19–23, 2016, Revised Selected Papers

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Center



Florian Wende
Zuse Institute Berlin

Be Part of the Conversation, Join the Community That's Right for You



Meet them at the
User Community Social

Tuesday, Nov 15

4:30pm - 6:00pm

Intel SC16 Booth, #1819



SC16

Salt Lake City, Utah | **hpc** matters.

Birds of a Feather Sessions

Optimizing Performance on Many-Core Processors: Unleashing the Power of the Intel® Xeon Phi and Beyond

(KNL clustering/MCDRAM mode discussion)

Wednesday, Nov. 16

12:15pm-1:15pm

Room 355-F



Omni-Path User Group (OPUG) Meeting

Thursday, Nov. 17, 2016

1:30pm-3:00pm

Room 155-A

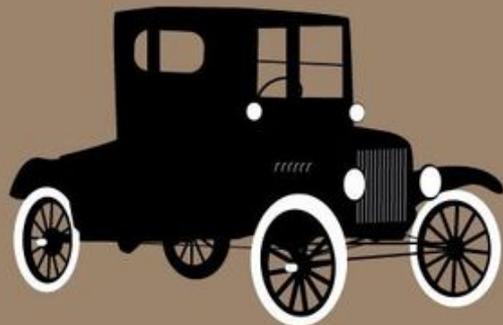


COMING TOGETHER IS A BEGINNING

KEEPING TOGETHER IS PROGRESS

WORKING TOGETHER IS SUCCESS

- Henry Ford



Become a member!
Host a regional meeting!

<http://ixpug.org>



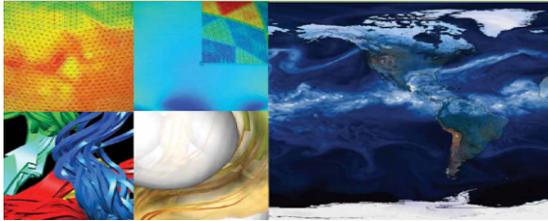
The Mission HPC Facility for DOE Office of Science Research



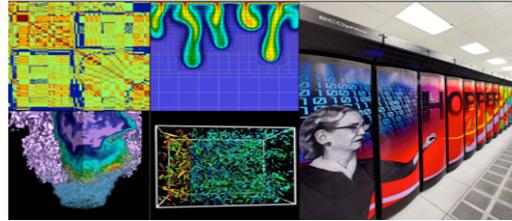
U.S. DEPARTMENT OF
ENERGY

Office of
Science

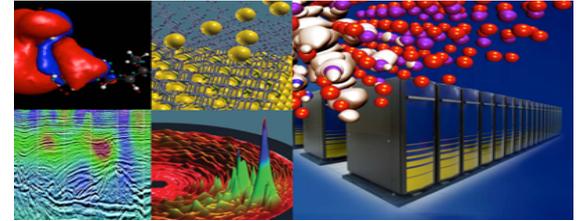
Largest funder of physical
science research in U.S.



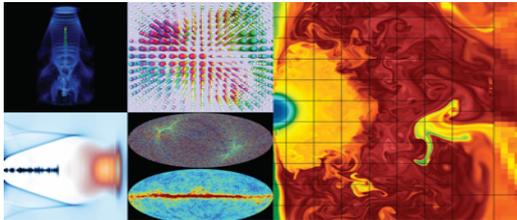
Bio Energy, Environment



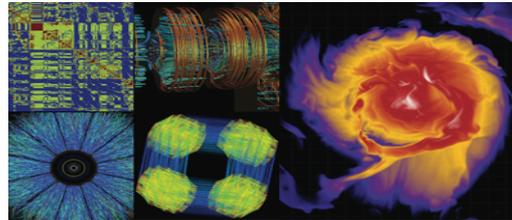
Computing



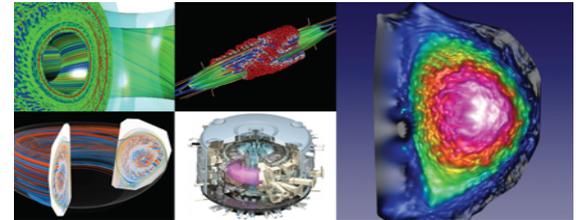
Materials, Chemistry, Geophysics



Particle Physics, Astrophysics



Nuclear Physics



Fusion Energy, Plasma Physics

6,000 users, 700 projects, 700 codes, 48 states, 40 countries, universities & national labs